Exhibit B

[redacted]

NT003US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/952,599
Filed	:	July 27, 2013
For	:	MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION
Examiner	:	SUN, MICHAEL
Art Unit	:	2184
Conf. No.	:	6784
Docket No.	:	NT003US

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December 31, 2014

(Date)

/Jamie J. Zheng/

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AMENDMENT RESPONSE TO OFFICE ACTION DATED APRIL 3, 2014

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Non-Final Office Action dated July 31, 2014, Applicant hereby submits the following amendment and remarks.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 7 of this paper.

Application Number: 13/952,599
Filed July 27, 2013

AMENDMENTS TO THE CLAIMS

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1. (Currently Amended) A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals;

memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and

a plurality of buffer circuits to receive the module control signals, ~~a~~ each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and

wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and

wherein ~~the plurality of buffer circuits are configured to align~~ the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group ~~groups~~ of memory devices ~~such that the read data signals are transmitted to the memory controller from the memory module substantially aligned with each other and~~ in accordance with the time interval

and a read latency parameter of the memory system during a memory read operation.

2. (Currently Amended) The memory module of claim 1, wherein each module control signal arrives at the plurality of buffer circuits at different points in time across more than one clock cycle of the system clock, and wherein the ~~plurality of buffer circuits are~~ each respective buffer circuit is configured to align the respective set of read data signals such that ~~they~~ different sets of read data signals corresponding to the memory read operation are transmitted by the different buffer circuits onto ~~to~~ different sets of data/strobe signal lines in the memory bus ~~controller~~ within one system clock cycle.

3. (Original) The memory module of claim 1, wherein each buffer circuit includes receiver circuits to receive corresponding ones of the module control signals, each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal, and wherein each buffer circuit further includes at least one signal adjustment circuit to adjust one or more the module control signals to mitigate any metastability condition in the module control signals.

4. (Currently Amended) The memory module of claim 1, wherein the module control device further receives the system clock from the system memory controller and transmits a registered clock signal to the plurality of buffer circuits, and wherein the each respective buffer circuit regenerates one or more clock signals from the registered clock signal and provides a regenerated clock signal to the respective group of memory devices.

5. (Currently Amended) The memory module of claim 1, wherein the respective ~~each~~ buffer circuit comprises:

a time interval determination circuit to receive, during a write operation, a first signal from the module controller and a second signal from the memory ~~controller~~ bus and to generate a delay signal indicating a time interval between the first signal and the second signal;

a delay circuit to delay the respective set of read data signals received from the respective group of memory devices ~~a signal in the buffer circuit~~ according to the delay signal ~~indicating the time interval, the signal in the buffer circuit being one of a read data signal, a read strobe signal, and a regenerated clock signal~~.

6. (Currently Amended) A method of operating a memory module in a memory system having a memory controller, the memory module being coupled to the memory controller via a memory bus, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module including memory devices and a module controller coupled to the memory controller via the set of control/address signal lines, the method comprising:

receiving a read command from the memory controller via the set of control/address signal lines;

generating module command signals and module control signals in response to the read command;

producing read data from the memory devices in response to the module command signals;

controlling a plurality of sets data paths in a plurality of data buffers using the module control signals such that each respective set of the plurality of sets of data paths receive and conduct a respective portion of the read data; and

outputting read data from the plurality of data paths ~~to~~ onto the memory bus, wherein a first set of the plurality of data paths output a first portion of the read data onto a first set of data/strobe signal lines in accordance with a first time interval, wherein a second set of the plurality of data paths output a second portion of the read data onto a second set of data/strobe signal lines in accordance with a second time interval different from the first time interval, the first time interval and the second time interval having been determined during a prior write operation performed in the memory system ~~controller, wherein at least one signal in each of the plurality of data buffers is delayed such that the read data output from the plurality of data paths are aligned with each other and in accordance with a read latency parameter of the memory system~~.

7. (Original) The method of claim 6, further comprising:

determining a metastability condition associated with a respective module control signal at each of the plurality of data buffers; and

adjusting the respective module control signal based on the metastability condition.

8. (Currently Amended) The method of claim 6, further comprising, in the each data buffer:

receiving at least one first module control signal generated in the memory module in

response to a write command associated with the prior write operation;

determining a time interval between receiving the at least one first module control signal and receiving a write signal associated with the write command from the memory controller, the write signal being one of a write data signal and a write strobe signal; and

delaying ~~the~~ at least one signal in the respective data buffer according to the time interval.

9. (Original) The method of claim 8 wherein the at least one signal is a clock signal.

10. (Original) The method of claim 8 wherein the at least one signal is at least one of a read data signal and a read strobe signal.

11. (Original) The method of claim 8, wherein the write signal is a write strobe signal, the method further comprising:

detecting a preamble of the write strobe signal to determine the time interval.

12. (Currently Amended) A buffer circuit for use in a memory module coupled to a memory controller via a memory bus, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module including a plurality of memory devices organized in groups and a module controller coupled to the memory controller via the set of control/address signal lines, comprising:

a time interval determination circuit to ~~receive, during a write operation, a first signal from the module controller and a second signal from the memory controller and to generate a delay signal indicating~~ determine a time interval between receiving a first signal from the module controller and receiving a second signal from the memory bus ~~the first signal and the second signal~~; and

a delay circuit to ~~delay at least one signal in the buffer circuit~~ time transmission of data/strobe signals received from a respective group of the plurality of memory devices to the memory controller via a respective set of the plurality of sets of data/strobe signal lines according to ~~the delay signal indicating~~ the time interval.

13. (Currently Amended) The buffer circuit of claim 12 wherein the buffer further comprises receiver circuits to receive corresponding ones of the module control signals, each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal ~~the at least one signal is a clock signal~~.

14. (Currently Amended) The buffer circuit of claim 12 wherein ~~the at least one signal is at least one of a read data signal and a read strobe signal~~ the buffer circuit further comprises at least one signal adjustment circuit to adjust one or more the module control signals to mitigate metastability condition in the module control signals.

15. (Original) The buffer circuit of claim 12, wherein the first signal is an enable signal to enable a write data path in the buffer circuit.

16. (Original) The buffer circuit of claim 15, wherein the second signal is a write strobe signal.

17. (Original) The buffer circuit of claim 15, wherein the second signal has a preamble, and wherein the time interval determination circuit includes a preamble detector to detect the preamble of the second signal.

18. (Currently Amended) The buffer circuit of claim 15 ~~18~~, wherein the time interval determination circuit further includes a counter to count a number of clock cycles between receipt of the first signal and detection of the preamble of the second signal.

19. (Currently Amended) The buffer circuit of claim 12, further comprising:

a clock regeneration circuit to receive a clock signal from the module controller and to regenerate a regenerated clock signal according to the ~~delay signal indicating the~~ time interval.

20. (Currently Amended) The buffer circuit of claim 12, wherein the buffer circuit is coupled to a respective ~~set~~ group of the plurality of memory devices on the memory module, and wherein the buffer circuit further comprises a clock regeneration circuit to receive a clock signal from the module controller and to provide a regenerated clock signal to the respective group of the plurality of memory devices.

REMARKS

This amendment responds to the non-final Office Action dated July 31, 2014, in which the Examiner:

- objected to certain informalities in claims 1-5;
- rejected claims 1-20 under pre-AIA 35 U.S.C. 102(e) as being anticipated by Manohararajah et al. (US 8,565,033), hereafter referred to as Manohararajah.

I. CLAIM AMENDMENT

Claims 1-2, 4-6, 8, 12-14, and 18-20 are amended. No new matter is added.

II. OBJECTION TO INFORMALITIES IN CLAIMS 1-5

Claim 1 has been amended and the term "substantially" has been removed. Therefore, the objection is now moot.

III. REJECTION OF CLAIMS 1-20 UNDER PRE-AIA 35 U.S.C. 102(E) AS BEING ANTICIPATED BY MANOHARARAJAH

Applicant disagrees with the Examiner's assertion that Manohararajah teaches a memory module comprising, among other things, "a plurality of buffer circuits to receive the module control signals from the module control device, a respective buffer circuit corresponding to a respective group of memory devices, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals." The interface circuitry 24 in Manohararajah, which the Examiner asserts to include the "buffer circuits", is part of the memory controller 10 (Manohararajah, FIG. 3). Thus, whatever "buffer circuits" the Examiner speculates could be part of the interface circuitry 24 are not even on the memory module and cannot possibly receive module control signals from any module control device on the memory module 22 or be controlled by at least one of the module control signals.

Applicant also disagrees with the Examiner's assertion that Manohararajah teaches "the plurality of buffer circuits" being distributed across a surface of the memory module 22. As shown in Manohararajah, FIG. 3, any buffer circuits that could be part of the interface circuitry 24 are not even on the memory module 22. They are separated from the memory module by the

memory bus including the signal lines 34-1 to 34-N and 36. So, they cannot be distributed across a surface of the memory module 22.

Applicant also disagrees with the Examiner's assertion that "the buffer circuitry being on the memory module itself or on the interface would be an obvious variant as the utility function is the same." This assertion is baseless. For a claim to be rejected under pre-AIA 35 U.S.C. 102(e), a single piece of prior art must disclose each and every claimed limitation. Persons of ordinary skill in the art will understand that there is clear difference between data buffers on a memory module and data buffers on a memory controller. The Examiner cannot make up what is lacking in the prior art by a simple assertion that it is obvious. Furthermore, claim 1 recited not just data buffers on a memory module, but data buffers that receive module control signals from a module control device on the memory module and are controlled by the module control signals. The Examiner has not shown how the interface circuitry 24 in Manohararajah can be controlled by any module control device on the memory module 22, as claimed in claim 1.

Claim 1 as amended includes further limitations not disclosed in Manohararajah. For example, Manohararajah does not teach or disclose data buffers coupled between respective groups of memory devices and respective sets of the plurality of sets of data/strobe signal lines in the memory bus and distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines. Further, Manohararajah also does not disclose that each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation, and is further configured to time transmission of a respective set of read data signals received from a respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

The Examiner cites Col. 7, lines 42-53, Col. 8, lines 51-67, and Col. 9, lines 1-18 Manohararajah in the Office Action, but these passages in Manohararajah merely states that the DQ/DQS signals can be delayed so that the DQ/DQS signals are phase aligned for optimal setup and hold times. Nowhere in Manohararajah it is described the transmission of read data signal from each respective buffer is timed in accordance with a time interval determined based signals

received by the each respective buffer. Thus, Manohararajah does not anticipate claim 1 as amended.

Therefore, claim 1 as amended is patentable over Manohararajah.

Claim 2 as amended, claim 3, claims 4-5 as amended depend from claim 1 as amended and include further limitations in addition to the limitations in claim 1. Therefore, claim 2 as amended, claim 3, claims 4-5 as amended are patentable for at least the same reasons claim 1 as amended is patentable.

Claim 6 as amended includes the limitations of:

> controlling a plurality of sets data paths in a plurality of data buffers using the module control signals such that each respective set of the plurality of sets of data paths receive and conduct a respective portion of the read data; and
>
> outputting read data from the plurality of data paths onto the memory bus, wherein a first set of the plurality of data paths output a first portion of the read data onto a first set of data/strobe signal lines in accordance with a first time interval, wherein a second set of the plurality of data paths output a second portion of the read data onto a second set of data/strobe signal lines in accordance with a second time interval different from the first time interval, the first time interval and the second time interval being determined during a prior write operation performed in the memory system.

These features in claim 6 as amended are not disclosed in Manohararajah because Manoahararajah does not teach or disclose a plurality of data paths for receiving and conducting read data from the memory devices, wherein the plurality of data paths are controlled by module control signals generated by a module control device on the memory module in accordance to a read command received via a set of control/address signal lines in the memory bus. As discussed above, the interface circuitry 24, wherein the Examiner speculated to include a plurality of data paths are not on the memory module 22 and could not possibly be controlled by module control signals generated by any module control device on the memory module 22 in accordance to a read command received via a set of control/address signal lines in the memory bus.

Manohararajah also does not teach or disclose the plurality of data paths outputting read data onto the memory bus. As shown in FIG. 3 of Manohararajah, the interface circuitry 24, being on the memory controller 10, cannot possibly output read data onto the memory bus. It can only receive read data from the memory bus. Furthermore, Manohararajah does not disclose the

additional features of a first set of the plurality of data paths outputting a first portion of the read data onto a first set of data/strobe signal lines in accordance with a first time interval, a second set of the plurality of data paths outputting a second portion of the read data onto a second set of data/strobe signal lines in accordance with a second time interval different from the first time interval, the first time interval and the second time interval being determined during a prior write operation performed in the memory system.

Therefore, claim 6 as amended is patentable over Manohararajah.

Claim 7, claim 8 as amended, and claims 9-11 depend from claim 6 as amended and include further limitations in addition to the limitations in claim 6 as amended. Therefore, claim 7, claim 8 as amended, and claims 9-11 are patentable for at least the same reasons claim 6 as amended is patentable.

The arguments regarding claim 1 as amended apply to claim 12 as amended. Therefore, claim 12 as amended is also patentable over Manohararajah.

Claims 13-14 as amended, claims 15-17, and claims 18-20 as amended depend from claim 12 as amended and include further limitations in addition to the limitations in claim 12 as amended. Therefore, claims 13-14 as amended, claims 15-17, and claims 18-20 as amended are patentable for at least the same reasons claim 12 as amended is patentable.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicants reserve the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicants have made any disclaimers or disavowals of any subject matter supported by the present application.

The Examiner is invited to call the undersigned at (650) 273-6008 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: December 31, 2014

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